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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/709,428

05/05/2004

Cheng-Yen Huang

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09/22/2005

EXAMINER

TRINH, HOA B

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION

P.O. BOX 506

MERRIFIELD, VA 22116

ART UNIT

PAPER NUMBER

2814

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/709,428

Applicant(s)

HUANG, CHENG-YEN

Examiner

Vikki H. Trinh

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 30 June 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 11, 19 and 27-32 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 11, 19 and 27-32 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. The request for continued examination of this application under 37 CFR 1.114 filed on June 30, 2005, is acknowledged. Claims 11, 19, and 27-32 are pending in this application.

### ***Specification***

2. The disclosure is objected to because of the following informalities: Applicant does not clearly describe a "first pin" and a "second pin" on the chip, and a "third bonding pad" connected to a second lead frame. The examiner suggests the use of consistent terminology throughout the disclosure and claims.

Appropriate correction is required.

### ***Claim Objections***

3. Claims 11, 19, 27, and 30 are objected to because of the following informalities: Because applicant does not clearly describe a first pin and a second pin in the specification, the examiner assumes that the first pin and second pin are the bonding pads positioned on the chip in claims 11, 19, 27 and 30. Also, in claim 11, line 3, "a package" should be "the package". In claim 27, line 3, "a package" should be "the package". Furthermore, in claims 11, 19, 27 and 30, it is not clear which bonding pad from the specification and/or drawings is the third bonding pad that connects to the second lead frame. Figure 6 shows the first lead frame and the second frame, but figure 6 does not show the lead frames connected to any bonding pads. The examiner assumes that first and second lead frames are the lead frames that connect to any one of the bonding pads, as shown in figure 4. Appropriate correction is required.

*Claim Rejections - 35 USC § 102*

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 11, 19, and 27-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Hara et al. (6,414,387) (hereinafter Hara).

Hara discloses, as to claim 11, a chip-packaging 11 (fig. 1) with bonding options 12, 13, 17, 15, 14, 7, 6, 5, 4, 16 (fig. 1) connected to a package substrate 10 (fig. 1, Note: Hara recites character 10 as a ground electrode which has the same function as a package substrate because it supports a chip 3), comprising the substrate 10 (fig. 1) ; a chip 3 (fig. 1) mounted on the substrate 10, the chip 3 comprising a plurality of bonding pads 4, 5, 6, 7, 14, 16 (fig. 1) , a first bonding pad 5 or 6 (fig. 1) directly contacting the substrate 10 ; a first lead frame 13 or 12 (fig. 1) connected to a second bonding pad 4 or 7 (fig. 1) through a first pin 4 or 7 of the chip 3; and a second lead frame 15 or 17 (fig. 1) connected to a third bonding pad 14 or 16 (fig. 1) through a second pin 14 or 16 (fig. 1) of the chip for receiving input signals to control the voltage level of the second pin 14 or 16. Note: the examiner assumes that the first pin and the second pin of the chip are the bonding pads on the chip.

As to claim 19, Hara teaches a method of packaging a chip having a bonding options 12, 13, 17, 15, 14, 7, 6, 5, 4, 16 (fig. 1) connected to a package substrate 10 (fig. 1, Note: Hara recites character 10 as a ground electrode which has the same function as a

package substrate because it supports a chip 3), comprising providing the substrate 10 (fig. 1) ; mounting a chip 3 (fig. 1) on the substrate 10, the chip 3 comprising a plurality of bonding pads 4, 5, 6, 7, 14, 16 (fig. 1) , connecting a first bonding pad 5 or 6 (fig. 1) directly to the substrate 10 ; connecting a first lead frame 13 or 12 (fig. 1) to a second bonding pad 4 or 7 (fig. 1) through a first pin 4 or 7 of the chip 3; and connecting a second lead frame 15 or 17 (fig. 1) to a third bonding pad 14 or 16 (fig. 1) through a second pin 14 or 16 (fig. 1) of the chip for receiving input signals to control the voltage level of the second pin 14 or 16. Note: the examiner assumes that the first pin and the second pin of the chip are the bonding pads on the chip.

As to claim 27, Hara discloses a chip packaging 11 (fig. 1) with bonding options 12, 13, 17, 15, 14, 7, 6, 5, 4, 16 (fig. 1) connected to package substrate 10 (fig. 1, Note: Hara recites character 10 as a ground electrode which has the same function as a package substrate because it supports a chip 3), comprising the substrate 10 (fig. 1) connected to either a high voltage or a low voltage; a chip 3 (fig. 1) mounted on the substrate 10, the chip 3 comprising a plurality of bonding pads 4, 5, 6, 7, 14, 16 (fig. 1) , a first bonding pad 5 or 6 (fig. 1) directly contacting the substrate 10 ; a first lead frame 13 or 12 (fig. 1) connected to a second bonding pad 4 or 7 (fig. 1) through a first pin 4 or 7 of the chip 3, the first lead frame 12 or 13 being connected to either a high voltage or a low voltage and the voltage level of the first pin 4 or 7 being the logical opposite of the voltage level of the substrate 10; and a second lead frame 15 or 17 (fig. 1) connected to a third bonding pad 14 or 16 (fig. 1) through a second pin 14 or 16 (fig. 1) of the chip 3 for receiving input signals to control the voltage level of the second pin 14 or 16. Note: the examiner

assumes that the first pin and the second pin of the chip are the bonding pads on the chip. Also, note that in order for the device to work or function, it has to be connected to some potential.

As to claim 28, Hara teaches that the high voltage may be a power supply and the low voltage may be a ground. (See fig. 1, col. 5, lines 33-40). Note that in order for the device to work or function, it has to be connected to some potential.

As to claim 29, Hara discloses that the substrate 10 (fig. 1) is connected to a power supply and the first lead frame 12 or 13 is connected to a ground (fig. 1).

As to claim 30, Hara teaches a method of a chip packaging 11 (fig. 1) with bonding options 12, 13, 17, 15, 14, 7, 6, 5, 4, 16 (fig. 1) connected to a package substrate 10 (fig. 1, Note: Hara recites character 10 as a ground electrode which has the same function as a package substrate because it supports a chip 3), comprising providing the substrate 10 (fig. 1) connected to either a high voltage or a low voltage (fig. 1, and col. 5, lines 20-40); mounting a chip 3 (fig. 1) on the substrate 10, the chip 3 comprising a plurality of bonding pads 4, 5, 6, 7, 14, 16 (fig. 1); connecting a first bonding pad 5 or 6 (fig. 1) directly to the substrate 10 ; connecting a first lead frame 13 or 12 (fig. 1) to a second bonding pad 4 or 7 (fig. 1) through a first pin 4 or 7 of the chip 3, the first lead frame 12 or 13 being connected to either a high voltage or a low voltage (col. 6, lines 55-60) and the voltage level of the first pin 4 or 7 being the logical opposite of the voltage level of the substrate 10 (fig. 1, Note that the pin 4 or 7 is connected to the output terminal on the power supply region 11 (fig. 1)); and connecting a second lead frame 15 or 17 (fig. 1) to a third bonding pad 14 or 16 (fig. 1) through a second pin 14 or 16 (fig.

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1) of the chip 3 for receiving input signals to control the voltage level of the second pin 14 or 16. Note: the examiner assumes that the first pin and the second pin of the chip are the bonding pads on the chip. Also, note that in order for the device to work or function, it has to be connected to some potential.

As to claim 31, Hara teaches that the high voltage may be a power supply (col. 6, lines 15-20) and the low voltage may be a ground (fig. 1, col. 6, lines 55-61). Note that in order for the device to work or function, it has to be connected to some potential.

As to claim 32, Hara discloses that the substrate 10 (fig. 1) is connected to a power supply (col. 6, lines 55-61) and the first lead frame 12 or 13 is connected to a ground (fig. 1). Note that in order for the device to work, it has to be connected to some potential.

### ***Response to Arguments***

6. Applicant's arguments with respect to claims 11 and 19 have been considered but are moot in view of the new ground(s) of rejection. New claims 27-32 fall with the new rejection of claims 11 and 19.

### **Conclusion**

Kinsman discloses a chip packaging method and device having a lead frame, substrate, chip, and bonding pads. See fig. 1B-1C.

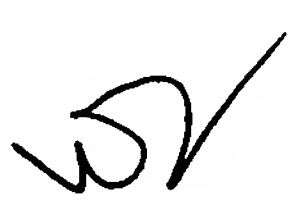
Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Vikki Trinh whose telephone number is (571) 272-1719. The Examiner can normally be reached from Monday-Friday, 9:00 AM - 5:30 PM Eastern Time. If

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attempts to reach the examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Wael Fahmy, can be reached at (571) 272-1705. The office fax number is 703-872-9306.

Any request for information regarding to the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Also, status information for published applications may be obtained from either Private PAIR or Public Pair. In addition, status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. If you have questions pertaining to the Private PAIR system, please contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

Lastly, paper copies of cited U.S. patents and U.S. patent application publications will cease to be mailed to applicants with Office actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site ([www.uspto.gov](http://www.uspto.gov)), from the Office of Public Records and from commercial sources. Applicants are referred to the Electronic Business Center (EBC) at <http://www.uspto.gov/ebc/index.html> or 1-866-217-9197 for information on this policy. Requests to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

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